Nano Transistors Performance Analysis

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ABSTRACT

Nanowire Transistors have attractive attention due to the feasible high performance and excellent controllability of device current. In this paper, the performance analysis of nanowire transistors made of different materials such as S ilicon (S i), Germanium (Ge), Gallium Arsenide (GaAs) and Indium Arsenide (InAs) are investigated. S elf-consistent 3D simulations are used due to their 3D distribution of electron density and electrostatic potential. The output characteristics of the nanowire transistors are studied in details for all the materials of different transport orientation. Nanowire, a 3D Poisson self-consistent simulator is used for simulation which can study the 3D transport in nanowire transistor considering phonon scattering based on the effective-mass approximation.

Keywords: Nanowire Transistor, NEGF, Coupled Mode Space, Uncoupled Mode Space, Crystal Orientation.

1. INTRODUCT ION

Nanowires are attracting much interest from those seeking to apply nanotechnology and especially those investigating nanoscience. Nanowire transistors are an emerging class of materials with great potential for applications in future electronic devices. Although conventional planar Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) are approaching nanometer scale, but their performance becomes limited by short channel effects, increasing OFF-state current and poor electrostatic control of the channel [1]. Unlike other low-dimensional systems, nanowires have two quantum- confined directions but one unconfined direction available for electrical conduction. This allows nanowires to be used in applications where electrical conduction, rather than tunneling transport is required. Because of their unique density of electronic states in the limit of small diameters, nanowires are expected to exhibit significantly different optical, electrical and magnetic properties to their bulk 3D crystalline counterparts.

Nanowires are nanoscale structures which are frequentlysingle crystal materials and are typically cylindrical in shape.They can be formed in a variety of materials including metallic(e.g., Ni, Pt, Au), semiconducting (e.g., Si, Ge, GaAs, InAs, InP,GaN, etc.), and insulating (e.g., SiO2 , TiO2), but are mostfrequently fabricated using semiconducting materials. Theyhave fascinated attention not only because of their extremelysmall size, but also their size causes new physics (quantumeffects) to apply. This does not occur classically which can causechanges in material properties [2]. Three phenomena that are themost notable are: (i) as the diameter of nanowire decreases, theenergy band gap can change, (ii) the diameter of nanowire canchange the material's character [3], and (iii) ballistic transport,i.e. without scattering, can occur which can lead to notablyimproved device performance

The reason which leads the researchers think aboutreplacement of planar MOSFET is Nanowire Transistor (NWT)that has the strongest gate control over planar MOSFET andother proposed structures. However, at this time the NWT stillis in its early stage, there is a lot of space to optimize the structureparameters and lots of new phenomenon to be explore by bothexperimental and computational approach, for instant, we needto determine the optimal diameter, the best material and theeffect of random dopant or surface roughness or p hononscattering on its performance. Figure 1 shows a schematic structureof a nanowire transistor showing metal source and drainelectrodes with the nanowire.

In this research, the output characteristics are studied bydifferent transport orientation (i.e., 100, 110 and 111) andvarying the oxide thickness in details for the NWT formed offour different semiconducting materials like Silicon (Si),Germanium (Ge), Gallium Arsenide (GaAs) and IndiumArsenide (InAs).

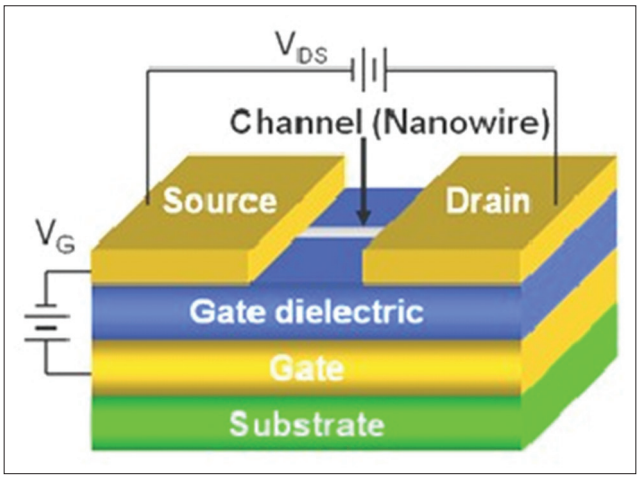

Figure 1: Schematic of a Nanowire T ransistor showing metal source and drain electrodes with the Nanowire

2. HOMOGENEOUS NANOWIRE BASED DEVICES

In the case of nanowires with homogeneous structure andcomposition, Silicon Nanowires (Si NWs) have mostextensively been studied [4]. This is due partly to thedominance of Si in the semiconductor industry, but also reflectsthe high-level of control of structure and doping demonstratedin fundamental Si NW growth studies [4-5]. Additionally, othernanowire materials such as Ge, GaAs, InAs, GaN, and metaloxides have also received broad attention [6-9].

A. Silicon Nanowires (Si NWs)

Researches on nanowires began to accelerate in 1998, whenSi NWs with diameters < 20 nm and lengths > 1 μm were demonstrated using a laser-ablation method [10]. The ability toprepare nanowires with diameters < 20 nm made it possible forthe first time to produce devices that could approach a 1D limitdesirable for high-performance transistors. Initial efforts led todemonstration of NWTs and basic devices configured usingcrossed nanowire geometry, including p-n diodes and bipolartransistors [11]. However, the electrical properties of nanowiresin these initial studies were far from optimal, for example-leading to low apparent carrier mobilities and large sample tosample variations. These studies thus underscored thesignificance of growth of nanowires with controlled material andelectrical properties.

B. Germanium Nanowires (Ge NWs)

Ge NW devices have also been studied by several groups[6], [12] & [13] due to the higher electron and hole mobilitiescompared with Si. Compared to Si NW, Ge NW devices areexpected to have smaller contact effects because the smaller Gebandgap will yield a lower Schottky barrier at the metal/NWinterface. For example, studies of p-type Ge NW devices withPd S/D contacts yielded a hole mobility of 600 cm2 /V.s [14]. Inaddition, complementary n-type and p-type Ge NW deviceswere demonstrated based on a surface doping approach toprevent uncontrolled sidewall deposition during the nanowiregrowth [12]. Prototype gate-all-around devices were alsodemonstrated by Zhang et al.[13] using atomic-layer depositionand magnetron sputtering to uniformly coat an Al2 O3 dielectriclayer and an Al gate layer. Compared with the back-gated GeNW devices, the gate-all-around devices showed excellentsubthreshold performance due to the improved electrostatics.The ON-state performance of these latter devices was lowerthan earlier studies due to the series resistance caused by thefinite positive (albeit small) Schottky barriers.

C. Gallium Arsenide Nanoeires (GaAs NWs)

To push that past limit, researchers are working on transistordesigns that rely on materials with better electrical propertiesthan silicon. Now researchers have made high-performancetransistors from a promising candidate material: GaAsnanowires. GaAs materials have higher charge mobility than Si,which should allow III/V transistors to switch ON and OFFfaster than silicon-based devices but the challenge is cost. GaAswafers are much more expensive and far smaller than siliconwafers, meaning manufacturers wouldn't be able to make asmany chips at once as they do with Si to keep chip costs down.NWs offer a way around the wafer problem, because they shoulduse less material. The growth of the wires is catalyzed by spotsof gold, patterned in a tight line by electron-beam lithographyonto a surface. As the chamber fills with gaseous precursors, thegold spots

catalyze the deposition of solid GaAs. By controllingthe ratio of gallium and arsenide, and conditions such astemperature and pressure, it is shown that the gold catalystmoves along the surface as the nanowire grows, rather thanleaving the surface and forming the nanowires vertically. Thenanowire arrays to make a type of high-performance transistorsimilar to those found in radar equipment and cell-phones. Each10-µm-wide transistor contains about 30 nanowires, along withthree electrodes. A top electrode called a gate applies a voltageacross the device to switch the nanowires between conducting,or "ON" and insulating, or "OFF" states. In the ON state,charges flow between source and drain electrodes. Thetransistors have blistering switching speeds, turning ON andOFF 75 billion times a second, or at 75 GHz. The previousrecord for planar nanowire transistors was 1.8 GHz. Researchersare also thinking that mobility of InAS is three times higher thanGaAs, so if it is possible to make and if it works, then we willget THz speeds.

D. Indium Arsenide Nanoeires (InAs NWs)

InAs nanowires have widely been studied as a building blockfor n-type FETs [14-16]. InAs is an attractive material fornumerous reasons. First, its small effective electron mass (0.023m0) results in high electron-mobility in bulk materials. Second,an electron gas layer is known to form at the surface of planarInAs due to Fermi level pinning in the conduction band. Third,the formation of an electron gas combined with the small bandgap of 0.35 eV should relatively yield transparent contacts toInAs nanowire devices. Studies of InAs NWTs have yieldeddepletion-mode n-channel FETs with electron mobilities on theorder 3000 cm2 /V•s [14-15]. The epitaxial growth of InAsnanowires have led to the demonstration of vertical nanowirestructures with a wrap-around gate with a low saturation voltageof 0.15 V [16]. In addition, the clean electron conductionchannel has led to the demonstration of quantum devicesincluding single-electron transistors and quantum dots inChemical Beam Epitaxy (CBE) grown InAs/InP nanowire axialhetero structures in which the InP layers serve as tunnel barriers[15].

3. METHODOLOGY

To deeply understand device physics of NWTs and to assesstheir ultimate performance limits, simulation work is necessaryand important. In contrast to a planar MOSFET, which has auniform charge and potential profile in the transverse direction(normal to both the gate and the source-to-drain direction), anNWT has a 3D distribution of electron density and electrostaticpotential. As a result, a 3D simulator is required for thesimulation of NWTs.

In this paper, a 3D self-consistent quantum simulation ofNWTs based on the effective-mass approximation (whosevalidity in then a scale device simulation has been established inRef. [20]) is proposed. The methodology of this work is shownas flowchart in Figure 2. The calculation involves solution of a self-consistent 3D Poisson equation for the electrostatic potential.After that, the calculation involves solution of a 2D Schrödingerequation with open boundary conditions for each cross sectionof the nanowire transistor to obtain the electron sub bands (alongthe nanowire) and Eigen functions . The 2D Schrödinger by a(coupled/uncoupled) mode space approach is solved whichprovides both computational efficiency and high accuracy ascomparedwithdirectrealspacecalculations.Coupled/Uncoupled Non Equilibrium Green Function (NEGF)transport equations is solved for the electron charge density.Phonon-electron interaction calculation is done with the self-consistent born approximation. First step is repeated to calculatethe electrostatic potential. If the self-consistent loop hasconverged, the electron current is calculated using the NEGFapproach.

Different transport models are implemented into simulator.In this paper, both ballistic NEGF model and dissipative NEGFmodel is discussed. Ballistic NEGF model gives the upperperformance limit of Si, Ge, GaAs and InAs NWTs, and adissipative NEGF model with a simple treatment of scatteringwith the Buttiker probes offers an efficient way to capturescattering in the quantum mechanical frame work.

A. Coupled Mode Space Approach

In this part of the work, the Coupled Mode Space (CMS)approach is briefly discussed and listed out the basic equationsfor the particular case of interest. In the 3D domain, the fullstationery Schrödinger equation is given by -

$$H_{3D}\,\psi(x,y,z) = E\,\psi(x,y,z) \quad (1)$$

Where, H3D is the 3D device Hamiltonian. Assuming anellipsoidal parabolic energy band with a diagonal effective-masstensor (for the case that the effective-mass tensor includes non-zero off diagonal elements), H3D is defined as -

$$H_{3D} = \frac{h_2}{\quad} \frac{\partial_2}{\quad}{}_2 - \frac{h_2 \partial}{\quad}(\frac{1\partial}{\quad}) \; {}_*2m_*(y,z)\,\partial x2\,\partial y\,m_y(y,z)\,\partial y_x$$

$$h_2\,\partial 1 \partial \quad (*) + U(x,y,z) \ldots . (2) - \quad 2\,\partial z\,m_z(y,z)\,\partial z \qquad (2)$$

Here, mx* , my * and mz* are the electron effective mass in the x, y,and z directions, respectively; U (x, y, z) is the electronconduction band-edge profile in the active device. After thedevice Hamiltonian H is obtained, the electron density andcurrent can be calculated using the NEGF approach. The NEGFapproach is a commonly used method for the simulation ofnanoscale electronic devices. The retarded Green's function ofthe active device is defined as -

G (E)=[E 潲 – H – ∑s (E) – $\sum_1$ (E) – $\sum_2$ (E)] −1 (3)

Here, ∑S is the self-energy that accounts for the scattering insidethe device (zero in the case of ballistic approach), and ∑1 (∑2) is the self-energy caused by coupling between device and thesource (drain) [20].

B. Uncoupled Mode Space Approach

The uncoupled mode space approach gives quantumconfinement and transport separately. In the simulation ofNWTs, it is assumed that the shape of the Si body is uniformalong the x direction. As a result, the confinement potential profile (in the yz plane) varies very slowly along the channel direction.

For instance, the conduction band-edge U(x,y,z) takes thesame shape but different values at different x. For this reason,the eigen functions ξ m(y,z; x) are 10 approximately the samealong the channel although the Eigen values Esub m(x) is different. So it is assumed,

ξ m(y, z; x) = ξ m(y, z) (4)

The retarded Green's function for mode m of the activedevice is rewritten as [20]

Gm(E) = [ESm – hmm – ∑m (E) – ∑m (E) –s1 $\sum_m$ (E)] −1...............................2 (5)

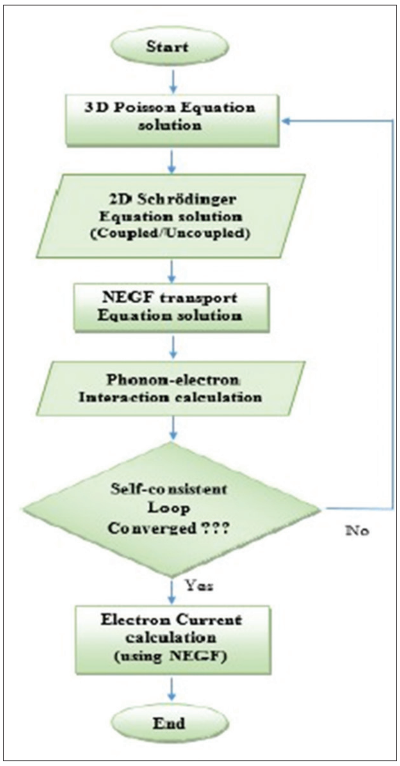

Figure 2: Methodology of this work.

C. NEGF Formalism

The simulation of electronic devices generally contains self-consistent solution of the electrostatic potential and carrierdistribution inside the device. Over the years, device engineershave improved our collective knowledge of carrier transportand semiconductor physics. Earlier treatment of electrons andholes as semi-classical particles with an effective mass wasgood enough to predict semiconductor device behavior and thedrift-diffusion equation was adequate to describe carriertransport.

MOSFETs have shrunk to nanoscale dimensions, whichhave required a re-examination of this approach to devicemodeling. A more sophisticated analysis of the device physicsis needed, such as the Non Equilibrium Green's Function(NEGF) approach, to model devices all the way to ballistic level(< 10 nm) [1][19]. The NEGF transport model is by far the mostrigorous method among existing quantum transport models andis the approach utilized in this modeling study.

4. SIMULAT ION RESULT S AND DISCUSSION

In this work, 3D "Nanowire" simulator is used for thesimulation of NWTs. The simulation software used for themodeling of nanowire transistors is based on the work done byHong-Hyun Park et al. and his colleagues at Purdue University[17-18].

A. Simulation

Because of longer simulation time, the uncoupled modespace NEGF transport is considered only. Although Si is themost common and economical material used in semiconductorindustry, it has some limitations and maybe reaches its physicalend soon. There are some other materials which are very activein research and exhibit some promising improvement over Si.Hence, the Si with other semiconductors for the nanowiretransistor channel material is compared. The gate work functionof 4.15 eV is used, which is for the metal Aluminium (Al). Thenanowire diameter is considered to be 4 nm, oxide thickness of SiO_2 is 1 nm, gate length is of 8 nm and the source-drainextension length is of 8 nm each. The doping profile of 2×1020 per cm3 is considered for the source-drain extensions.The channel region doping is set to zero which provides resultssimilar to that of an intrinsic channel.

The gate voltage is kept fixed at 400 mV and the draincurrent is extracted for different drain bias by using Si as thechannel material with uncoupled mode space approach. Thesame thing is repeated by using Ge, GaAs and InAs as thechannel material.

Figure 3 represents Drain Current (Id) vs. Drain Voltage (Vd)plot of nanowire transistor for four different materials (Si, Ge,GaAs, and InAs) with Uncoupled mode space approach for 100crystal orientations. Here the nanowire transistor Ge, GaAs andInAs as channel material has more ON current when comparedwith that of the Si counterpart for crystal orientation "100" withuncoupled mode transport.

Drain Current (Id) vs. Drain Voltage (Vd) plot of nanowiretransistor for four different materials (Si, Ge, GaAs, and InAs)with Uncoupled mode space approach for crystal orientations"110" is shown in Figure 4.

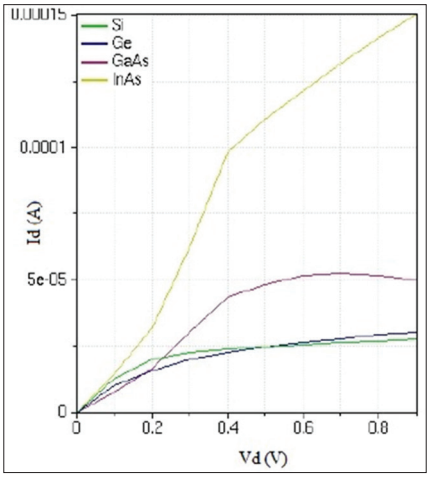

Figure 3: Drain Current (Id) vs. Drain Voltage (Vd) plot of nanowire transistor for four different materials (Si, Ge, GaAs, and InAs) with uncoupled mode space approach for 100 crystal orientations

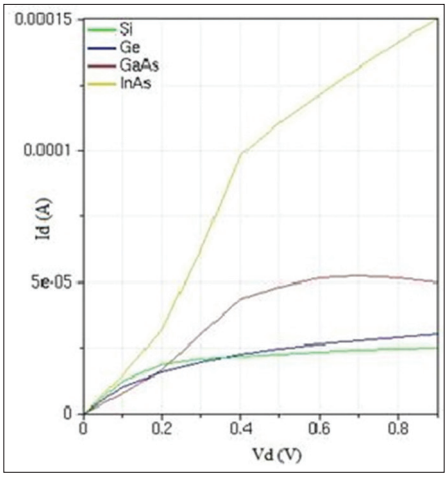

Figure 4: Drain Current (Id) vs. Drain Voltage (Vd) plot of nanowire transistor for four different materials (Si, Ge, GaAs, and InAs) with Uncoupled mode space approach for 110 crystal orientations.

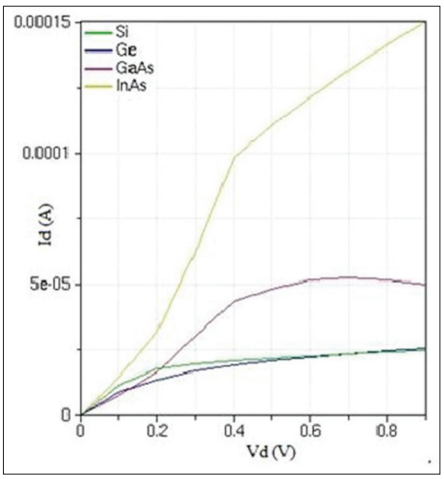

Figure. 5: Drain Current (Id) vs. Drain Voltage (Vd) plot of nanowire transistor for four different materials (Si, Ge, GaAs, and InAs) with Uncoupled mode space approach for 111 crystal orientations

Figure 5 also represents Drain Current (Id) vs. Drain Voltage(Vd) plot of nanowire transistor for four different materials (Si,Ge, GaAs, and InAs) with Uncoupled mode space approach butdifferent crystal orientations “111”.

It is inferred from the above Figure 3, 4 and 5 that the nanowiretransistor Ge, GaAs and InAs as channel material has more ONcurrent when compared with that of the Si counterpart forvarious crystal orientations (100, 110 and 111) with uncoupledmode transport. From the analysis of the different material’sNWTs, the orientation of 110 has less ON current comparedwith orientation of (100 and 111) for Si material. Ge, GaAs andInAs has almost same ON current in all the crystal orientations.

4. CONCLUSION

In this paper, the performance analysis of nanowiretransistors made of different materials such as Si, Ge, GaAs andInAs are investigated. The output characteristics of thenanowire transistors are studied in details for all the materialsof different transport orientations i.e.- 100, 110 and 111. Si hasless ON current in crystal orientation 110, but comparativelymore ON current in crystal orientation 100 and 111. Ge, GaAsand InAs all have more ON current than conventional Si in allthe crystal orientations and almost same ON current in all theorientations. InAs has the highest ON current in all the crystalorientations. For different orientation of mode space approach,Ge, GaAs and InAs NWTs give better performance thanconventional Si NWTs. So, conclusion can be drawn that Ge,GaAs and InAs have NWTs have higher mobility than Si NWTsand InAs has the highest mobility.

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